

Fig. 11. The whole workflow of Parmesan.

APPENDIX A SYSTEM-LEVEL IMPLEMENTATION

We implement Parmesan with PyTorch [29], Numba [30], and NetworkX⁵. The core of Parmesan contains around 12k lines of Python. In this section, we will introduce other components in Parmesan. To simplify the notation, we will use the word *optimizer* to denote the whole optimization process (including partitioning and mapping).

Fig. 11 describes the whole workflow of Parmesan. Given a DNN model written in PyTorch [29], our graph extractor will first conduct just-in-time (JIT) tracing and automatically extract the *operator-level computation graph*. We will then launch the profiler to profile the operator attributes (including forward/backward time/memory) and compute the total parameter size of this operator (allreduce time is highly correlated to the parameter size).

As for the *device topology*, we first measure the point-to-point (p2p) communication overhead between every pair of devices. Then, the device topology representation, a p2p bandwidth look-up-table (LUT), is constructed based on the postal model [26], [27].

After building the operator-level computation graph and the device topology LUT, our optimizer will take them as input and output the partitioning and mapping results.

Parmesan's *pipeline scheduler* and *simulator* evaluate the quality of the output solution and provide valuable information for further development. Inspired by FlexFlow [11], we develop a task-graph-based simulator to tackle the general device topology simulation problem. For the real-world evaluation, we design a GPipe [13] fashion pipeline scheduler in PyTorch 1.10.1 [29] with CUDA 11.3, and adopt NCCL 2.10.3 [31] distributed backend for both the p2p communication between pipeline stages and allreduce between the stage replicas. Note that the Python code snippets executed by our pipeline scheduler are automatically generated from the operator-level graph and the optimized solution.

Besides, Parmesan supports writing/reading computation graphs, device topologies, and optimized solutions. Thus, one can further explore some more optimization algorithms/flows and evaluate their performance based on Parmesan. Meanwhile, Parmesan's optimizer and simulator are independent of the deep learning framework. Provided the computation graph extracted by other DL frameworks (like Tensorflow [32]), Parmesan can automatically conduct model partitioning and device mapping for the given network and simulate the solution performance.

⁵https://networkx.org/

TABLE X Runtime (in seconds) of device mapping with different (S, R) and device topologies. P2P and allr refer to our two instantiations of device mapping respectively.

Topology	Alg.	(2, 8)	(4, 4)	(8, 2)	(4, 16)	(8, 8)	(16, 4)	(4, 64)	(8, 32)	(16, 16)	(4, 128)	(8, 64)	(16, 32)
2d mesh	p2p allr	19.8 0.4	0.6 0.9	4.0 0.4	605.5 1.3	908.1 1.5	908.0 1.6	609.7 611.4	762.0 6.4	762.0 48.7	- -	-	- -
2d torus	p2p allr	0.2 10.1	0.6 0.4	3.8 0.5	454.3 1.6	605.8 1.4	605.8 1.8	609.8 480.3	761.5 6.9	761.9 6.9	-	-	-
3d mesh	p2p allr	-	-	-	605.4 42.5	756.7 1.6	756.7 1.6	-	-	-	616.8 661.1	769.9 88.0	770.8 57.6
3d torus	p2p allr	-	-	-	325.2 1.7	454.9 1.5	756.9 1.7	-	-	-	617.0 82.1	618.9 15.5	619.2 36.5
random_blk_1	p2p allr	50.5 869.4	12.1 12.0	234.4 9.7	1379.4 905.4	1357.2 1021.5	490.7 760.1	345.9 911.0	607.8 910.5	608.1 910.7	354.1 925.0	1221.5 922.6	1223.5 923.3
random_blk_2	p2p allr	1057.8 906.7	1209.3 304.3	1119.9 3.0	455.9 908.0	757.5 1361.2	1208.4 646.7	1212.8 1402.3	1063.8 1086.3	1214.5 931.3	1221.8 1842.8	1223.6 1091.0	1224.6 1096.0
uniform_dist	p2p allr	681.7 185.5	320.7 453.9	478.2 0.6	987.0 644.7	781.1 454.1	1096.9 303.1	949.0 368.1	1251.4 217.6	1402.7 350.7	1282.5 334.9	1410.3 205.8	1541.0 208.6

TABLE XI

Comparison on results quality of device mapping with timeout heuristic to that of the optimal version (i.e., without the timeout heuristic). Figures in the table are the obtained objective values of Problem (5) for each combination of algorithm and (S,R). Differences are underlined. "*" denotes failure in obtaining results within 2 hours. "tmo" is short for timeout.

Topology	Alg.	(2, 8)	(4, 4)	(8, 2)	(4, 16)	(8, 8)	(16, 4)	(4, 64)	(8, 32)	(16, 16)	(4, 128)	(8, 64)	(16, 32)
2d mesh	p2p w/ tmo p2p opt	177625 177625	98940 98940	60715 60715	105340	66200	48829	105340	85851	114891		-	- -
	allr w/ tmo allr opt	169473 169473	81709 81709	47752 47752	82287 82287	47789 47789	28622 28622	86123	47766 *	28927 28927	-	-	-
2d torus	p2p w/ tmo p2p opt	177625 177625	98940 98940	60715 60715	104140	62067 60715	46091 39691	105340	85851 *	79498 *	-	-	-
	allr w/ tmo allr opt	169473 169473	81618 81618	47752 47752	82287 82287	47763 47763	28622 28622	82455 82455	47794 47794	28927 28927	-	-	-
3d mesh	p2p w/ tmo p2p opt				104140	64715 60715	47691 39691	-			105340	85851 *	65356
	allr w/ tmo allr opt	-	-	-	82287 82287	47763 47763	28622 28622	-	-	-	82483 82483	47830 47830	28978 28978
3d torus	p2p w/ tmo p2p opt	-	-	-	104140	63424 60715	47691 *	-	-	-	105340	81195	46091 *
	allr w/ tmo allr opt	-	-	-	82287 82287	47789 47789	28622 28622	-	-	-	82483 82483	47795 47795	28978 28978
random_blk_1	p2p w/ tmo p2p opt allr w/ tmo allr opt	7848025 7848025 2717063 2717063	5561027 5561027 359296 359296	5983883 5983883 96651 96651	7067273 * 2757132 *	5329127 * 123523 *	5285295 * 44337 *	10617386 * 2891041 *	10335205 * 1933769 *	11163700 * 2238277 *	10661165 * 2913360 *	11511750 * 1964333 *	14437823 * 2312136 *
random_blk_2	p2p w/ tmo p2p opt allr w/ tmo allr opt	1926463 * 737258 *	2274920 * 127727 127727	1542303 * 49239 49239	2340990 * 604081 *	1728740 * 63963 *	1770727 * 42814 *	3728927 * 1196374 *	3112257 * 661812 *	7265727 * 462752 *	3728927 * 1797052 *	3582268 * 1090929 *	7308867 * 561108 *
uniform_dist	p2p w/ tmo p2p opt allr w/ tmo allr opt	256915 * 184743 184743	267108 266651 102645 *	187708 187708 49154 49154	254602 * 106767 *	196161 * 56403 *	201261 * 40923 *	255566 * 107532 *	314564 * 57963 *	313764 * 44909 *	253809 * 107609 *	447725 * 58195 *	484707 * 45580 *

APPENDIX B

IMPACT OF TIMEOUT HEURISTIC OF DEVICE MAPPING ON RUNTIME AND QUALITY

As mentioned in Section V, a timeout heuristic is applied to speedup the searching during device mapping. In this paragraph, we make inspections on its runtime and resulted optimization quality. We conduct experiments on mapping the partitioned SemanticFPN on non-regular topologies (including grid-based and randomly generated topologies) under different (S,R) pairs. Table X shows the runtime of two instantiations of our device mapping. Our mapping algorithm successfully generates results for up to 512 devices within 40 minutes. Table XI illustrates the result quality generated by mapping with timeout by comparing them with the optimal version (i.e., without the timeout heuristic). For the cases of the grid-based topologies with the number of devices $D = S \times R \le 16$, the searching equipped with timeout is able to produce identical min-max stage time as by the optimal version. However, due to the increasing complexity, the optimal version fails to obtain the solution within 2 hours while our device mapping with timeout heuristic successes. "-" in Table X and Table XI denotes the number of devices $D \in S \times R$ cannot form a specific torus/mesh architecture.